

Comparison of fault ride through characteristics of VSI current controllers

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Abstract. The paper compares the voltage sag ride-through response of three current control methods applied to a voltage source inverter (VSI): traditional hysteresis, constant frequency (Dead-Beat) and hysteresis vector control with predictive algorithm.

In the analysis of these control methods it has been taken into account: response speed, current error deviation and total harmonic distortion during the sag, finding out the most suitable, depending on the required characteristics.

Key words: wind energy, voltage dips, current control, power quality.

1. Introduction

The growing use of renewable energy sources for the generation of electrical energy makes necessary the compliance with some technical requirements to prevent disturbing the operation of the grid that they are connected to.

These technical connection requirements affect all the aspects related to the quality of the energy sent to the grid [1] and in particular the behaviour of the system when it faces utility disturbances. Some of these problems are voltage dips due to short-circuits, and Spanish operation procedure P.O. 12.3 defines the expected behaviour of these installations when they face a voltage dip.

The paper compares the behaviour of three current control methods applied to a Voltage Source Inverter (VSI). These methods are: traditional hysteresis, constant frequency vector control (Dead-Beat) and hysteresis vector control with predictive algorithm at switching frequencies of 100 and 200 kHz.

2. Current control methods applied to a voltage source inverter

The traditional hysteresis control [2] is the simplest current control method, while being the one that shows better dynamic behaviour, good reference tracking and its implementation does not require knowing all the parameters of the circuit.

These controllers compare the reference currents i_a^* , i_b^* and i_c^* , and the real currents i_a , i_b and i_c , obtaining the current error in each phase ε_a , ε_b and ε_c and generating the switching signals independently, using a hysteresis comparator in each phase. When the error in any phase goes beyond the allowed value, the commutation takes place in this phase, trying to reduce this error.

In this method, the switching state of the bridge is obtained independently for each phase and thus, in systems where the neutral is not accessible, the influence among the phases causes the error not to be limited to its expected value.

Vector controllers obtain the switching state of the bridge by using an error phasor, considering the inverter as a global element and solving the problem of interaction among phases.

The results presented in this paper correspond to a constant frequency predictive controller, called Dead-Beat [3], one of the most frequently used. Its operation is based on obtaining the voltage reference at time k , \vec{V}_k^* , that makes the current error, $\vec{\varepsilon}_{k+1}$, to be as close as possible to zero at the end of the switching period. To do this, initially the value of the reference current at the end of the switching \vec{I}_{k+1}^* period is predicted from its previous values $\vec{I}_{k+1}^* = f(\vec{I}_k^* \dots \vec{I}_{k-n}^*)$. Next, \vec{V}_k^* is predicted using a function that models the inverter $\vec{V}_k^* = f(\vec{I}_{k+1}^*, \vec{I}_k, \vec{V}_k)$, where \vec{V}_k and \vec{I}_k are the values of the voltage and current at the inverter's output at instant k .

The second vector control analyzed is a predictive algorithm hysteresis control implemented in α - β coordinates [4]. It is based on a table controller, where the switching state is chosen according to the conditions stated in a dynamic table that is calculated each time the phasor error reaches the limit of the allowed band, using the actual parameters of the circuit at this time.

3. Ride through requirements in wind installations

According to operation procedure P.O. 12.3 “Requisitos de respuesta frente a huecos de tensión de las instalaciones eólicas” (Fault ride through requirements for wind installations), all the components of the installation must stand, without disconnection, voltage dips at the point of common coupling (PCC) when voltage level remains inside the shaded area of figure 1.

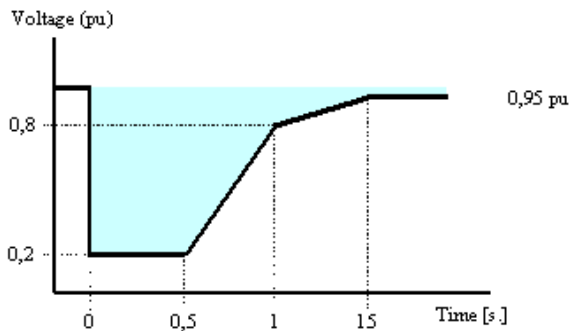


Fig. 1. Voltage (p.u.) – time curve for a voltage dip, according to P.O. 12.3.

The simulations presented in this paper show the system response to three-phase balanced faults, where the consumption of active or reactive power is not allowed, except for some exceptions, and the system must supply the maximum possible reactive power.

4. Dynamic behaviour when facing a voltage dip

In the simulations that have been carried out, the DC bus voltage is kept constant, and the utility voltage is reduced to a 20 % of its rated value, while supplying rated current. Besides, a variation of the current phase reference is applied in order to generate reactive power as soon as the voltage dip occurs ($t = 40\text{ms}$) considering that dip detection is instantaneous.

Figure 2 show that voltage error reaches 0.77 p.u. and recovery time is quite short, 1.7 ms.

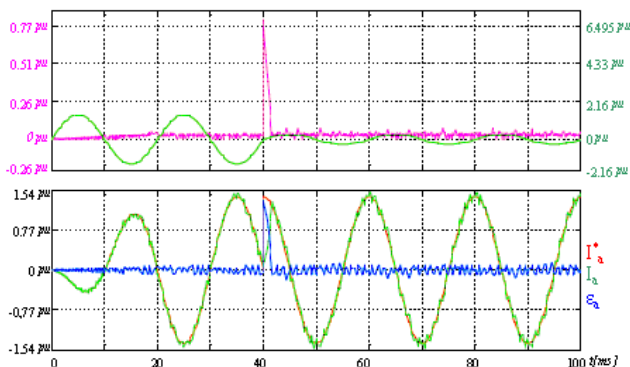


Fig. 2. Hysteresis controller. Phase A voltage (green) and total current error (pink). Current reference (red), actual current (green) and current error (blue).

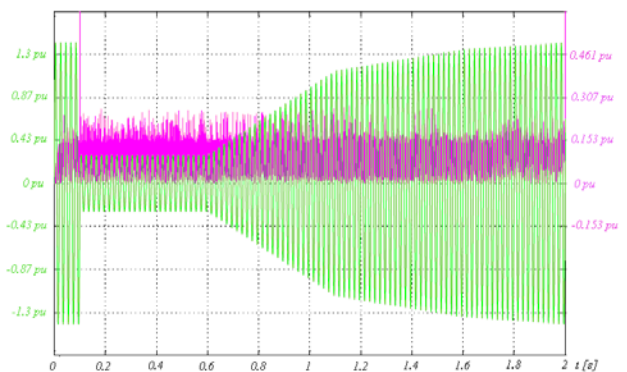


Fig. 3. Hysteresis controller. Phase A voltage (green) and total current error (pink).

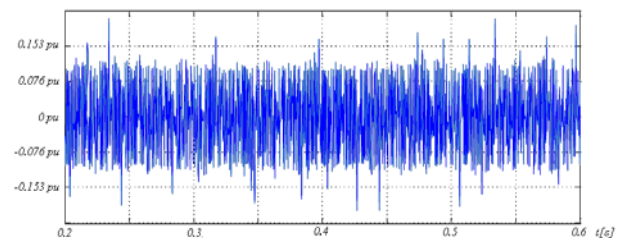


Fig. 4. Hysteresis controller. Phase A current error.

It can be noticed that current error is kept below 0.12 p.u., surpassing this value only during short duration pulses.

Average THD during the dip is 0.059, equal to the one existent before the fault, although during the recovery period this value rises to 0.071. Frequency increases slightly due to the increment in voltage difference between the DC bus and the grid, reaching 495 Hz.

For the predictive algorithm hysteresis vector control, operating at $f_m=100\text{ kHz}$ or 200 kHz the results are very similar to the previous case.

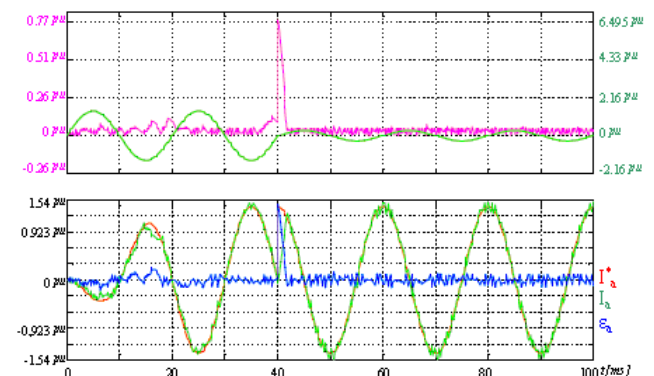


Fig. 5. Predictive algorithm hysteresis controller. Phase A voltage (green) and total current error (pink). Current reference (red), actual current (green) and current error (blue).

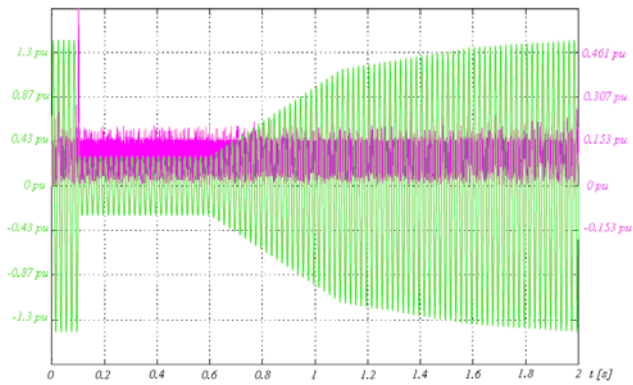


Fig. 6. Predictive algorithm hysteresis controller (100 kHz). Phase A voltage (green) and total current error (pink).

In the case of the predictive algorithm, the average THD during the dip worsens, going from 0,049 to 0.054 for a 200 kHz sampling frequency, and to 0,057 for a 100 kHz sampling frequency. During the recovery period THD is even worse, reaching approximately 0.068 in both cases.

There is also a significant increment in switching frequency, being 1140 Hz and 1070 Hz for $f_s = 100$ kHz and $f_s = 200$ kHz respectively.

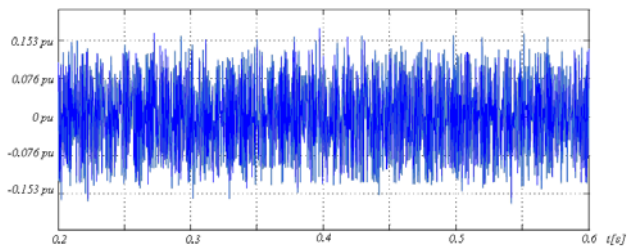


Fig. 7. Predictive algorithm hysteresis controller (100 kHz). Phase A current error.

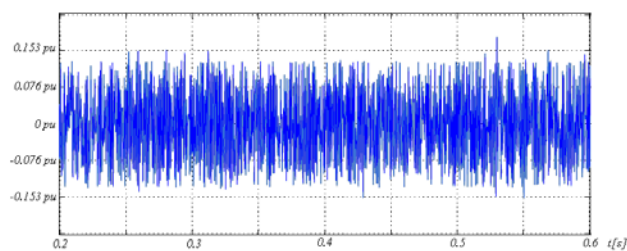


Fig. 8. Predictive algorithm hysteresis controller (200 kHz). Phase A current error.

Figures 7 y 8 show phase A current error and it can be noticed that using a 200 kHz sampling frequency causes an improvement in the error but in both cases the result is worse than the one obtained for the traditional hysteresis control. This is due to the fact that traditional hysteresis performs and independent control of each phase.

For the constant frequency controller (Dead-Beat), a switching frequency similar to the one in the predictive controller has been used, being 1070 Hz, for $f_s=200$

kHz, and 1140 Hz for $f_s=100$ kHz. The chosen frequency has been 1050 Hz.

Figure 9 shows that the current error reaches a maximum that surpasses 1 p.u. and the recovery of the system takes 6 ms, being the slowest method.

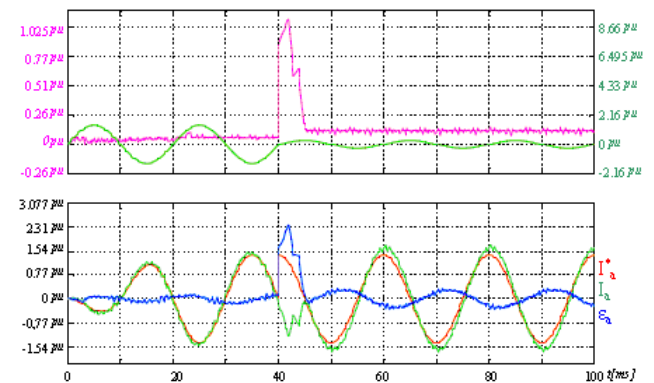


Fig. 9. Dead-Beat controller. Phase A voltage (green) and total current error (pink). Current reference (red), actual current (green) and current error (blue).

The THD obtained in steady state is 0.03, being the lowest of all the simulated methods. However, as can be seen in the following figures, the current error is much higher, reaching twice the previous value.

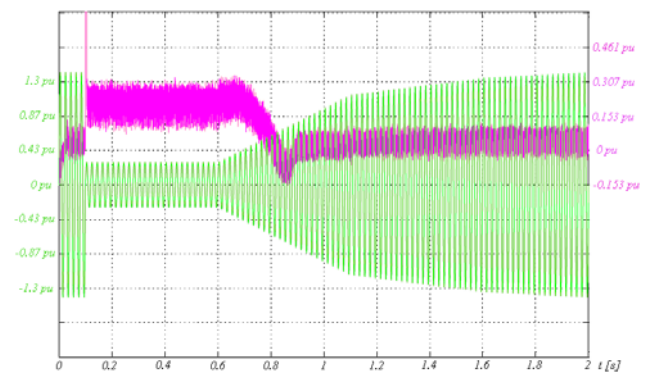


Fig. 10. Dead-Beat controller. Phase A voltage (green) and total current error (pink).

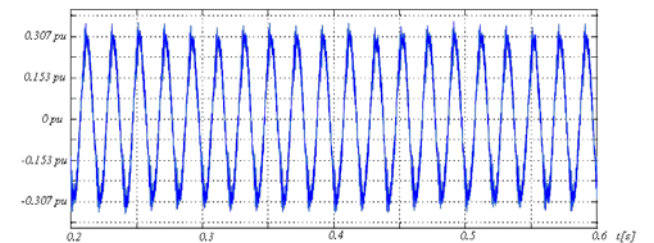


Fig. 11. Dead-Beat controller. Phase A current error.

The following figures show the evolution of utility current phasor and current error phasor from $t = 0.38$ ms to $t = 0.58$ ms.

Figure 12 shows the evolution of the current phasor just before the dip (green) and during the dip (red), going back to the new current reference, due to the phase shift imposed to the current reference in order to supply the required reactive power, according to the operation procedure.

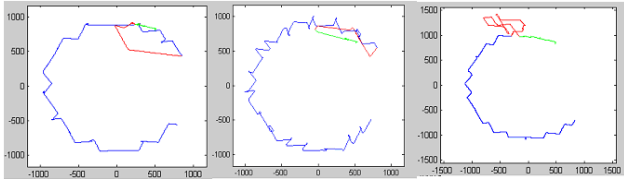


Fig. 12. Grid current phasors for the hysteresis, 100 kHz predictive algorithm and Dead-Beat controllers.

It can be noticed that the one going further from the reference during the transient and taking longer to recover is the Dead-Beat control, causing the error phasor to reach a high value. It can be observed in more detail in figure 13, which shows the evolution of the error phasor of the three methods. The first two plots, corresponding to the traditional hysteresis controller and the predictive algorithm controller are quite similar, being slightly better the second one. The plot showing a worse behaviour is the one corresponding to the Dead-Beat controller.

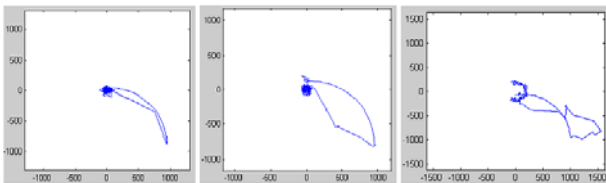


Fig. 13. Current error phasors for the hysteresis, 100 kHz predictive algorithm and Dead-Beat controllers.

Conclusions

It has been shown that both the hysteresis and the predictive algorithm methods respond quickly to the required current reference change, while keeping the value of harmonic content, being better the one shown by the predictive algorithm.

Switching frequency increases slightly, being lower for the traditional hysteresis control. Hysteresis band could be reduced to have a switching frequency similar to the one of the other cases and verify that the THD is reduced.

For the Dead-Beat control, the reference change response is slower and the error is larger. However, the harmonic content is much lower than for the other controls for the chosen switching frequency (1050 Hz).

References

- [1] S. A. Papathanassiou; N. D. Hatziargyriou. "Technical Requirements for the Connection of Dispersed Generation to the Grid". Power Engineering Society Summer Meeting, 2001. IEEE Volume 2, 15-19 July 2001 Page(s):749 - 754 vol.2
- [2] D.M.E Ingram, S.D.Round. "A fully digital hysteresis current controller for an inductive power filter". International Journal of Electronics, 1999, Vol 86, N° 1217-1232.
- [3] Rodriguez, J.; Pontt, J.; Silva, C.; Cortes, P.; Amman, U.; Rees, S.; "Predictive current control of a voltage source inverter" . Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual Volume 3, 20-25 June 2004 Page(s):2192 - 2196 Vol.3
- [4] J. F. Sanz, J. Sallán, M. A. Alonso, M. Sanz, J. L. Villa. "Development of a low-harmonic vector hysteresis current controller". ICREP 2006.