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Simulated 1200V SiC-MOSFET short-circuit behavior

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Abstract. This paper presents experimental measurements and simulated results of Silicon Carbide (SiC) MOSFETs on short-circuit operations. The main objective is to validate power transistor TCAD model, and its reliability to be representative of real components behavior (from static and dynamic characterization, to failure mechanisms). SENTAURUS simulation software could allow us to define not only 1200V SiC MOSFET itself but also other electronics components to develop a complex driving circuit. Results of simulation will help us to understand short-circuit effect on the component structure.

Key words

1200V SiC MOSFET, short-circuit, device simulation, failure mechanisms

1. Introduction

The evolution of aircraft is heading towards all-electrical systems (while limiting the use of pneumatic and hydro-electric energies). This implies smarter power management systems, justifying the need to use Solid State Power Controllers (SSPC).
These systems aim is to ensure the electrical distribution to aircraft's equipment and protect in case of overcurrent failures. SSPC are based on power semi-conductors having to withstand current and voltage of supplied equipment, and be able to detect and protect the aircraft in case of short-circuit occurrence on the power line.
Aircraft manufacturers are interested in silicon carbide (SiC) power transistor performances, able to replace actual silicon-based power modules (in order to increase the power density of SSPC) [1].
We based our work on the investigations made on short-circuit behavior of SiC MOSFETs [2]. Studies shown that these power transistors are able to withstand and limit an overcurrent during a predefined period, until the energy exceeds a critical value, causing a deterioration of gate oxide, resulting by a short-circuit between gate and source.

This failure also trains two different behaviors for drain-source junction, resulting in an open circuit (safe case) or in a short circuit (unsafe case) between drain and source.
These tests have been performed on three different 1200V SiC-MOSFETs references in our facilities (Figure 1&2). Table I shows our results (SC: Short Circuit, OP: Open Circuit). We can observe that ROHM component got the largest critical time (T_crit) and energy (E_crit). It also presents an Open Circuit (OC) behavior between drain and source after critical short-circuit test (contrary to CREE and ST components). In all cases, gate-source junction behavior confirms the analysis that gate oxide is the weakest point of this component [3].

Table I. - SiC MOSFET failures after short-circuit (V_{DS}=600V, V_{GS}=-5/20V, gate resistance Rg=47Ω)

	CREE	ROHM	STMicroelectronics
T_crit [µs]	9	13	7
Imax [A]	238	270	273,6
E_crit [J]	0,763	1,37	0,88
Drain-Source Failure	SC	OC	SC
Gate-Source Failure	SC	SC	SC

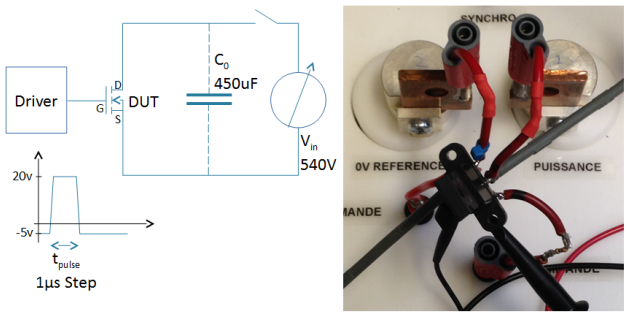

Fig. 1 a) Test bench synopsis b) device under test [4]

Figure 2 represents a short-circuit test performed on CREE 1200V MOSFET. The short circuit has been applied to the component during X+1µs pulse (V_{GS}=-5/20V, Rg=47Ω), with a Drain-Source voltage of 600V. Between each pulse, a rest period of 2 minutes was respected and a health test has been performed, to ensure that the component was still functioning. From 1 to 9µs, the component responded well to both short-circuit and health test.

The next step of 10µs pulse was fatal to the component. During the pulse ①, the current raised to a maximum value I_{Dmax}=237A, then was limited by the component. Once the Gate voltage get back to -5 volts ②, the component withstand 3µs in a degraded mode, V_{GS}=-5V as wanted but with a leakage current I_D=20A. After this time to failure (t_fail), both Drain-Source and Gate-Source junction were in a short circuit failure mode (I_{Dfail} > 700A).

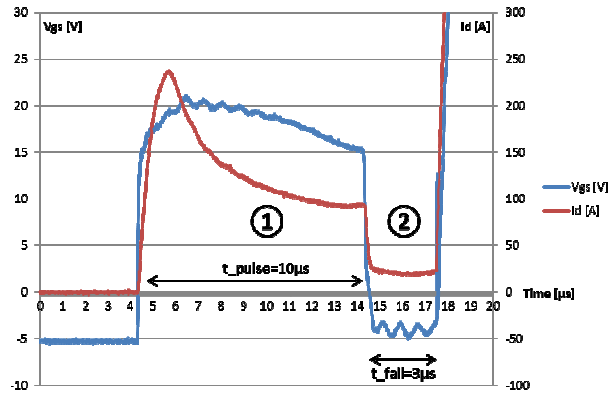

Fig. 2. CREE 1200V MOSFET C2M0080120D short-circuit test, V_{GS} & I_D behavior (@ V_{DS}=600V, V_{GS}=-5/20V, gate resistance Rg=47Ω)

2. Structure Modeling

In order to understand these transistors failure mechanisms and define guidelines for SSPC dimensioning, we developed our own SiC MOSFET model in SENTAURUS TCAD Synopsis Suite, based on a 1200V MOSFET manufactured by CREE [4]. Figure 3 shows our reverse engineering analysis.

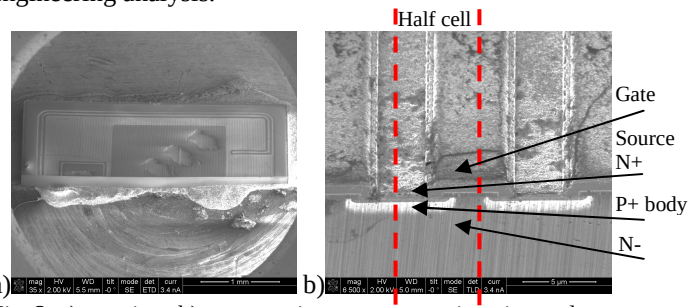

Fig. 3. a) top view, b) cross section, reverse engineering and SEM measurements of C2M0080120D [4]

These investigations help us to define an accurate structure for our 1200V SiC MOSFET model. Figure 4 presents an half MOSFET cell (drain contact isn't visible on this focus).

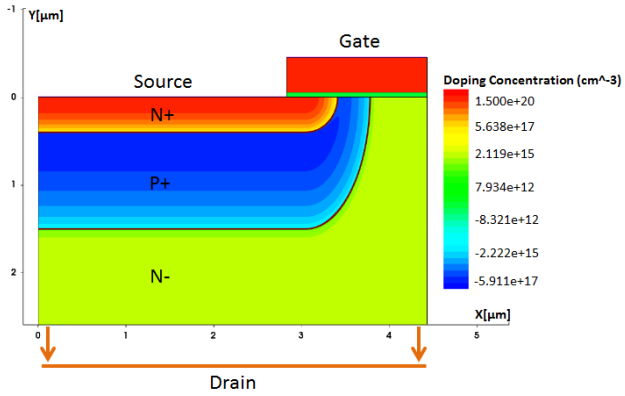

Fig. 4. 1200V SiC MOSFET half-cell

Thanks to the reverse engineering analysis, the geometrical part of the CREE 1200V SiC MOSFET has been defined. The next modeling step was to refine and adapt doping concentration of the Source region, the P-body region and drift layer. The main objective was to fit with static and dynamic characterization of the real component. Table II shows the datasheet, real, and simulated electrical characteristics of C2M0080120D MOSFET.

Table II. – Comparison of CREE 1200V SiC MOSFET electrical characteristics, datasheet, measured and simulated component

C2M0080120D	$V_{GS(th)}$ [V]	Vbr [V]	$R_{DS(on)}$ [mΩ]	t_{ON} [ns]	t_{OFF} [ns]
Datasheet	2.6	1200	80	31	42
Measured	3.1	1800	76	30	30
Simulated	3.8	1170	84	24	58

To date, the most difficult characteristic to reach between measured and simulated component is the breakdown voltage Vbr. We tried to parametrize several of doping concentration level, but it didn't seem conclusive.

The next step was to add interface traps between Oxide (SiO_2) and Silicon Carbide in the Gate area. These traps impact the MOSFETs characteristics [5]. The more charges there are at the interface, the more current leakage is observed in the off-state (reduction of breakdown voltage Vbr). At the same time, Gate threshold voltage $V_{GS(th)}$ is also impacted, reducing if interface traps charges increase.

Finally, the structure could not be complete if we did not take into account the thermal model of the component. This aspect remains the most difficult to implement, since SENTAURUS software didn't provide SiC model parameters. We tried to develop our own thermal model, in order to fit with the real component behavior. The most efficient method would be to recreate the conditions of the short circuit and observe simulated component behavior [6].

3. Results and discussion

Once this structure characterized to fit to the best, both static and dynamic, behavior of real component, we simulated two short-circuit operation on the model

(V_{GS}=0/20V, tpulse=30µs, $t_{ON/OFF}$=500ns with V_{DS}=600V & 1000V).
Figure 5 shows us two different behaviors for I_D in the first millisecond of the test. In both case, the short-circuit reach high current level, but for the V_{DS}=1000V, I_D current presents a failure behavior.

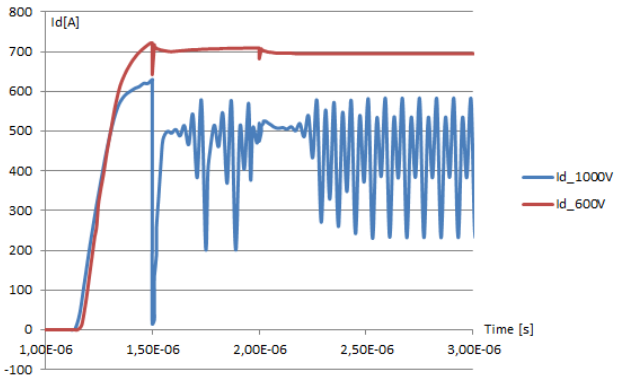

Fig 5. I_D in short-circuit-simulation with V_{DS}=600V and 1000V

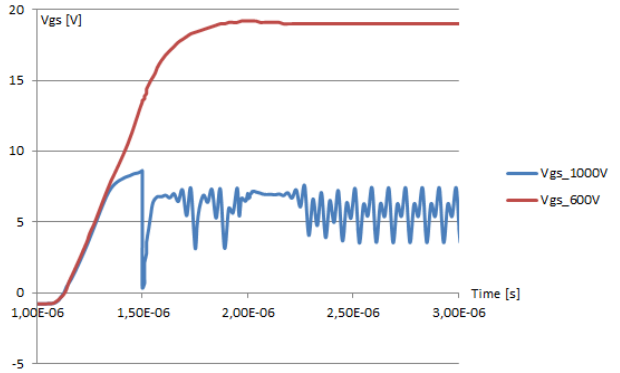

Fig. 6. V_{GS} in short-circuit simulation with V_{DS}=600V and 1000V

This failure state could also be visualized by looking at V_{GS} chart (Figure 6). In 600V case (red), gate voltage seems to follow the expected voltage. On the other side, in 1000V case, gate voltage shows us a failure mechanism, making us think of a leakage on gate contact.
TCAD simulation tool allow us to visualize state of the structure, with different parameters, at predefined times. Figure 7 and 8 show current density in the structure and the flow of the current (vectors). We can see that a reverse current is flowing from the channel zone to the gate oxide in both cases but at different level. Current density in oxide is higher @V_{DS}=1000V, explaining V_{GS} curve behavior (Figure 6).

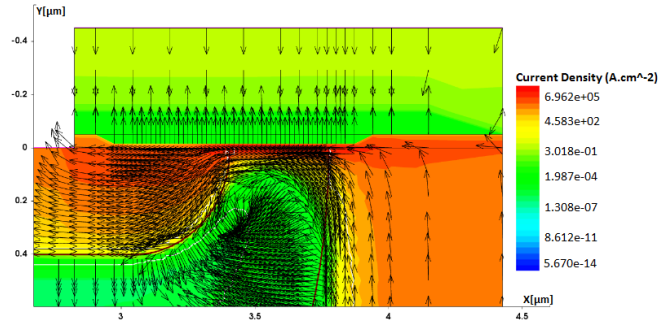

Fig. 7. Structure current density @tpulse=2.5µs and V_{DS}=600V

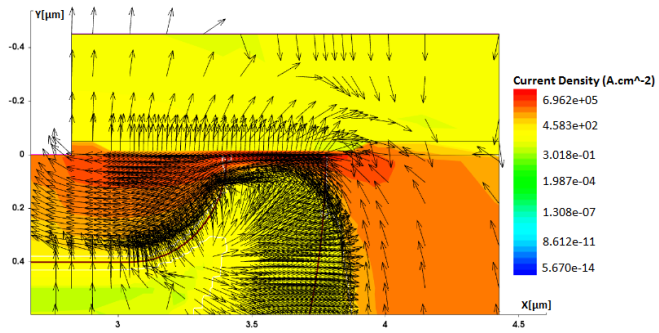

Fig. 8. Structure current density @tpulse=2.5µs and V_{DS}=1000V

As we can observe on bellow figures, current density seems to be the right indicator to analyze failure mechanisms. The next step will be to improve both thermal model and interface traps definition. Once the simulated short-circuit behavior will fit to the tested device, the simulated component would be representative of the real 1200V SIC MOSFET.

4. Conclusion

SENTAURUS simulation software allows us to understand failure mechanisms origins in SiC power MOSFET short-circuit operation. These results will help us to define an optimal application guideline to use these components as circuit breaker for aircraft application (SSPC). We developed a 1200V SiC MOSFET based on a component manufactured by CREE. The simulated component is almost representative of the real one, but there is still a need to refine the thermal model of the device.
Once this part will be optimized, the simulated component will be totally functional, and could predict the electrical and thermal behavior of the device in a custom electrical circuit. The analysis will also take into account the effects of traps at the Silicon Carbide and SiO_2 interface.

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