Renewable Energy, Environment, and Power Quality Journal (REE&PQJ)
ISSN:3020-531X
Volume 26, July 2026

Current Control Capability of the AC/DC Converter

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Abstract. This paper presents a comparative study of five hysteresis-based current-control algorithms applied to a grid-connected voltage source inverter operating as a bidirectional AC/DC converter. A linearized analytical model of the inverter–grid system, based on a current-generator representation of the intermediate DC circuit, is used to derive closed-form relations between phase currents, displacement angle and power factor. The algorithms — analog comparators, periodically sampled comparators, delta-modulation sampling, double hysteresis zones, and longest-operating-time vector selection — are characterized by switching count, T_{max}/T_{min} ratio, average DC current and total harmonic distortion (THD). Simulation results show THD between 0.26 % and 0.60 % at switching counts ranging from 549 to 1344 transitions per period. Experimental verification was carried out on 6.1 kW and 50 kW induction machines with control implemented on a TMS320C25 DSP. The results confirm the validity of the model and provide quantitative guidelines for algorithm selection.

Key words. Current control; mathematical model; hysteresis algorithm;; vector.

1. Introduction

Power electronics play an essential role in controlling and regulating the transfer of electricity from renewable and alternative energy sources to the consumers. Numerous static converter topologies have been proposed for photovoltaic systems over time. The topologies in these applications such as voltage source inverters (VSIs) as well as DC-DC converters are still developed and reviewed [1, 2]. Remarkable and capable solutions of microinverters VSIs and single phase converters connected directly to the grid are presented in various papers [3, 4, 5, 6, 7]. This large assortment of simple converters and more complex ones are created in newer technologies.
Converter topologies are generally divided into two groups: voltage-source inverters (VSIs) and current-source inverters (CSIs) [8, 9]. Recent technological advances have renewed research interest in the group of current-source inverters (CSIs) although research works on current control of voltage source inverters have a long history [10, 11]. However, CSI research still lags behind its voltage counterparts in terms of topology, modulation, and control.
The article presents some examples of how a current-controlled voltage source inverter (VSI) operates. Three different hysteresis algorithms designed for VSI control were selected. They use analytical expressions to describe the mathematical model of the VSI. The model defines and expresses in simplified formulas all the basic physical variables of the inverter and their mutual relationships: phase current and voltage, the shift angle between them, the power factor and the voltage of the intermediate circuit. It also allows to describe all the modes of electricity conversion in the full range of changes in the coefficient . The detailed description of the model was presented in [12]. Some results of these studies including current and voltage waveforms and control vectors are presented in the following figures.

2. Mains converter

A. Model of mains converter
It is assumed that VSI works as a mains converter. The analytical and simulation tests of the applied hysteresis control algorithms of the mains converter have been carried out based on the auxiliary mains converter model shown in Fig.1. Compared to the standard model of DC/AC inverter, it differs in the structure of the intermediate circuit, in which the ideal supply voltage source U_D is replaced by two elements: capacitance C and current generator G. The G generator is the source of current I_G which value and direction are determined by the converter load. The generator has zero internal conductivity. The intermediate circuit voltage U_D is equal to the capacitor voltage U_C. Three ideal keys K_a, K_b, K_c are able to simulate the operation of the inverter. They allow load switching between the poles of the supply voltage U_D. On the supply network side, there are three phase chokes with inductances L_a, L_b, L_c and resistances R_a, R_b, R_c. The voltages e_a, e_b, e_c are the phase voltages of the network, while the voltages u_{ab}, u_{bc}, u_{ca} stand for the interphase voltages. The symbols I_{0a}, I_{0b}, I_{0c} represent the values of phase currents at a selected time t_n. Subscripts a, b, c denote phases; k is the index of the active vector. Then,

with the vector k attached, the voltages u_{ak}, u_{bk}, u_{ck} and interphase voltages $u_{abk}, u_{bck}, u_{cak}$ are, correspondingly, the phase and interphase voltages at output terminals of the converter.

For the state shown in Fig.1, k = $100_2 = 4_{10}$. The model defines 8 switching states (k = 0,1,..7), each corresponding to a vector V_k. If it is assumed that the vector k is attached, then in the adopted converter model the phase equation a is of the form:

$$\boldsymbol{L_a \cdot \frac{di_a}{dt} + R_a \cdot i_a + e_a - u_{ak} = 0} \quad (1)$$

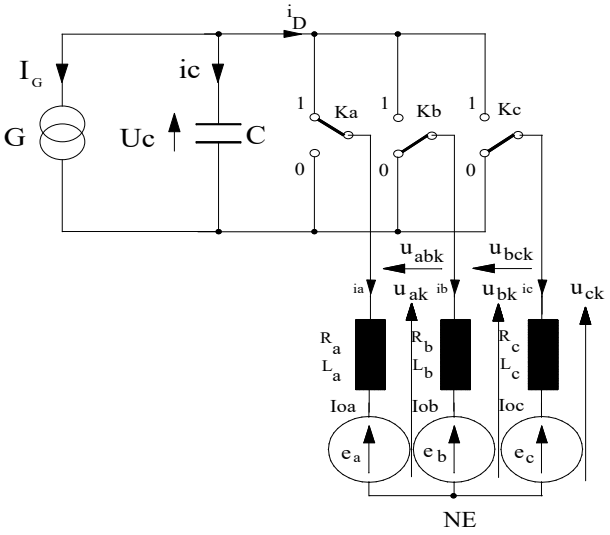

Fig.1. Model of PWM mains converter

Then, the equation describing the model of an ideal converter can be written as a matrix equation in the form corresponding to the notation of phase a.

$$\boldsymbol{L \cdot \frac{dI}{dt} + R \cdot I + E = 0} \quad (2)$$

Where the matrix I is the transposed matrix of phase currents $I = [i_a, i_b, i_c]^T$ and the matrix $\boldsymbol{E}$ is the transposed voltage matrix $E = [e_a - u_{ak}, e_b - u_{bk}, e_c - u_{ck}]^T$.

$\boldsymbol{L} = [L_a, L_b, L_c]^T$ is the inductance matrix and $\boldsymbol{R} = [\boldsymbol{R_a}, \boldsymbol{R_b}, \boldsymbol{R_c}]^{\boldsymbol{T}}$ – the resistance $\boldsymbol{R}$.

The interphase voltages u_{abk}, u_{bck} and phase voltages u_{ak}, u_{bk}, u_{ck} of the converter are calculated from voltage $U_D = U_C$ and take the values shown in Tables 1 and 2.

Table 1. Interphase voltages $\boldsymbol{u_{abk}, u_{bck}}$ for individual vectors $\boldsymbol{V_k}$

$\boldsymbol{V_k}$	$\boldsymbol{V_0}$	$\boldsymbol{V_1}$	$\boldsymbol{V_2}$	$\boldsymbol{V_3}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$	$\boldsymbol{V_6}$	$\boldsymbol{V_7}$
$\boldsymbol{u_{abk}}$	0	0	$\boldsymbol{-U_D}$	$\boldsymbol{-U_D}$	$\boldsymbol{U_D}$	$\boldsymbol{U_D}$	0	0
$\boldsymbol{u_{bck}}$	**0**	$\boldsymbol{-U_D}$	$\boldsymbol{U_D}$	**0**	**0**	$\boldsymbol{-U_D}$	$\boldsymbol{U_D}$	0

Table 2. Phase voltages for individual vectors V_k

$\boldsymbol{V_k}$	$\boldsymbol{V_0}$	$\boldsymbol{V_1}$	$\boldsymbol{V_2}$	$\boldsymbol{V_3}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$	$\boldsymbol{V_6}$	$\boldsymbol{V_7}$
$\boldsymbol{u_{ak}}$	**0**	$\boldsymbol{-\frac{U_D}{3}}$	$\boldsymbol{-\frac{U_D}{3}}$	$\boldsymbol{-\frac{2}{3}U_D}$	$\boldsymbol{\frac{2}{3}U_D}$	$\boldsymbol{\frac{U_D}{3}}$	$\boldsymbol{\frac{U_D}{3}}$	**0**
$\boldsymbol{u_{bk}}$	**0**	$\boldsymbol{-\frac{U_D}{3}}$	$\boldsymbol{\frac{2}{3}U_D}$	$\boldsymbol{\frac{U_D}{3}}$	$\boldsymbol{-\frac{U_D}{3}}$	$\boldsymbol{-\frac{2}{3}U_D}$	$\boldsymbol{\frac{U_D}{3}}$	**0**
$\boldsymbol{u_{ck}}$	**0**	$\boldsymbol{\frac{2}{3}U_D}$	$\boldsymbol{-\frac{U_D}{3}}$	$\boldsymbol{\frac{U_D}{3}}$	$\boldsymbol{-\frac{U_D}{3}}$	$\boldsymbol{\frac{U_D}{3}}$	$\boldsymbol{-\frac{2}{3}U_D}$	**0**
$\boldsymbol{u_{NE}}$	**0**	$\boldsymbol{\frac{1}{3}U_D}$	$\boldsymbol{\frac{1}{3}U_D}$	$\boldsymbol{\frac{2}{3}U_D}$	$\boldsymbol{\frac{1}{3}U_D}$	$\boldsymbol{\frac{2}{3}U_D}$	$\boldsymbol{\frac{2}{3}U_D}$	**0**

The voltage $\boldsymbol{U_C}$ changes as a result of the process of charging and discharging capacitor C. Capacitor current $\boldsymbol{i_C}$ depends on the current of the generator $\boldsymbol{i_G}$ and the current of the intermediate circuit $\boldsymbol{i_D}$: $\boldsymbol{i_C = -(i_D + i_G)}$. Therefore, the voltage $\boldsymbol{U_C}$ is given by the expression

$$\boldsymbol{u_C(t) = \frac{1}{C}\int_0^t -(i_D + i_G)\, d\tau + U_{C0}} \quad (3)$$

B. Structure of control systems

Given below is a brief description of the studied control algorithms and block diagrams of systems implementing them.

A1. Hysteresis algorithm with analog comparators

The object of tests was the control system shown in Fig. 2. The error is defined as the difference between the set current and the measured current:

$$\boldsymbol{\delta_i = i^*(t) - i(t)} \quad (4)$$

The phase error signals $\delta_a, \delta_b, \delta_c$ are given to the inputs of the analog comparators with hysteresis characteristics. In all three phases, the hysteresis zone has the identical value H. At the outputs of the comparators, digital signals are obtained, state 1 or state 0 is attributed depending on their level. A control variable in the form of a binary number $(k_a k_b k_c)$ is constructed from these signals. Based on this variable, the decision block selects an inverter vector V_k according to the principle $k = (k_a k_b k_c)$, where k is a decimal number with the value corresponding to the binary number $(k_a k_b k_c)$. In the stationary coordinate system α-jβ, the 3D inverter output voltage vector V_k assigned to this number has the form:

$$\boldsymbol{V_k = \frac{2}{3} U_D e^{j k_l \frac{\pi}{3}}} \quad (5)$$

where: k_l is the position angle coefficient of vector V_k relative to the coordinate system α-jβ. It is usually assumed that the direction of vector V_4 is consistent with the axis of real component, and then the coefficient k_l is assigned to the next vector k according to Table 3. The coefficient k_l is not determined for the vectors $\boldsymbol{V_0}$ and $\boldsymbol{V_7}$.

Table 3. Coefficients $\boldsymbol{k_l}$ of vectors $\boldsymbol{V_k}$

$\boldsymbol{V_k}$	$\boldsymbol{V_1}$	$\boldsymbol{V_2}$	$\boldsymbol{V_3}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$	$\boldsymbol{V_6}$
$\boldsymbol{k_l}$	4	2	3	0	5	1

Thus, the selection of vector V_k depends on the location of the current error vector δ_i in the complex plane sector which is determined by the control variable. For two control variable states: (000) and (111), the zero output voltage vector is activated $V_k = 0$.

Algorithm **A1** does not introduce restrictions on the inverter switching speed. However, taking into account the capabilities of the simulation program, discretisation of the control process was introduced which consisted in sampling the current with maximum frequency of 1 MHz. In real systems, analog comparators can change the initial state in the time below 1μs, and the applied simulation model does not reproduce well this property. However, compared to object parameters, the assumed sampling period can be considered sufficiently short and the results obtained in this way reliable.

A2. Hysteresis algorithm with comparators activated periodically. The object of the simulation was the control system shown in Fig. 3. The converter is controlled according to the hysteresis algorithm based on the solution of algorithm A1. However, the error signals are activated here with constant frequency at the inputs of the analog comparators. The sampling period is selected taking into account dynamic properties of the object to avoid excessively high inverter switching frequencies. The algorithm was tested for the time $\boldsymbol{T_p = 100\ \mu s}$. In the other solution, the control variable $(k_a k_b k_c)$ can be activated periodically at the decision block input, as shown in Fig. 3, while the phase currents are measured continuously. This model was selected for further studies. Vector V_k is selected following the same principle as for algorithm A1.

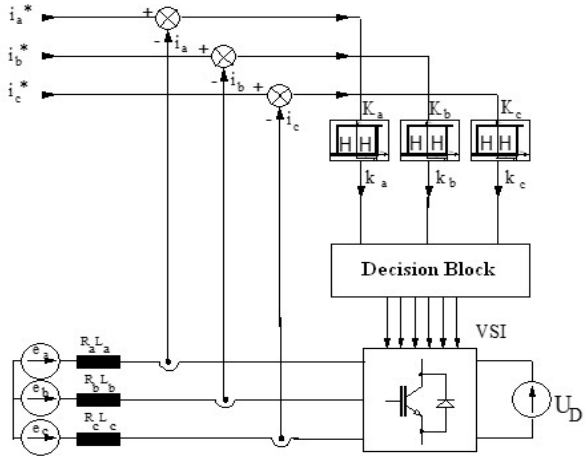

Fig.2. Control system with three analog error comparators

Notably, the hysteresis zone width must be correlated with the sampling frequency and load time constant: excessive reduction of the hysteresis zone degrades rather than improves inverter operation.

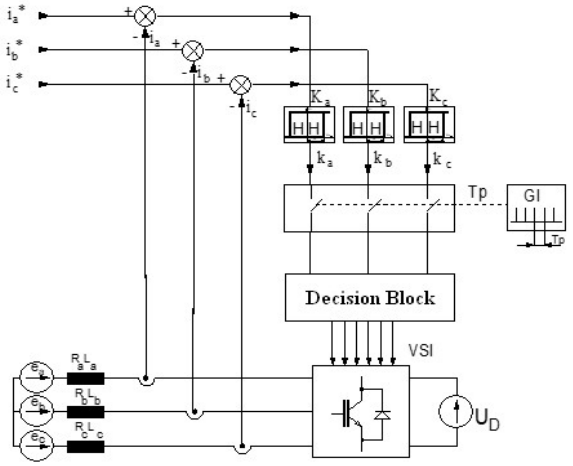

Fig.3. Control system with three error comparators activated periodically

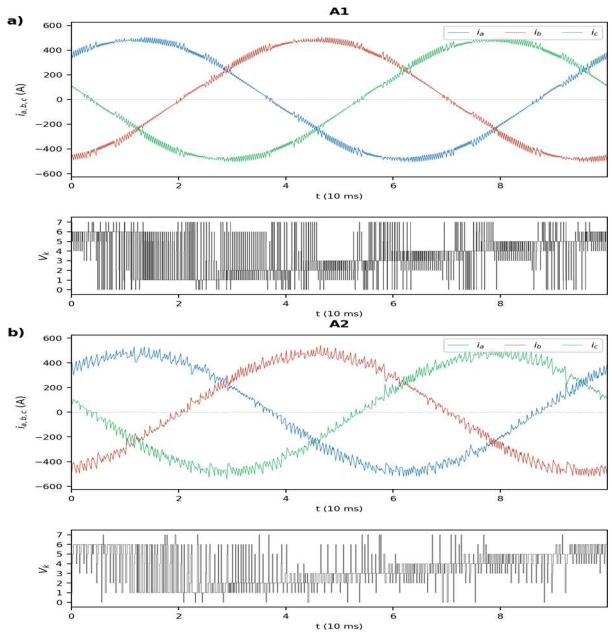

Fig.4. Waveforms of inverter phase currents and voltage vectors for hysteresis algorithms A1 (a) and A2 (b).

A3. Hysteresis algorithm with sampling

This algorithm is a variation of a type of control algorithms called delta modulation algorithms. The principle of operation of this algorithm is based on a concept proposed in [17]. This algorithm has two important features. The first of them is the principle of periodic sampling of phase currents, while the second is the tendency to activate zero vectors as often as possible.

The phase current error $\delta_i = i^*(t) - i(t)$ is compared with the set error zone $\boldsymbol{H}$, after which the following decision-making procedure is executed:

- if $\lceil \delta_i \rceil > \boldsymbol{H}$ then the non-zero vector is activated,
- if $\lceil \delta_i \rceil < \boldsymbol{H}$ then the zero vector is activated.

Non-zero vectors are selected when the error exceeds zone H; once the error re-enters the zone, the zero vector requiring the fewest switch transitions is applied.

A4. Hysteresis algorithm with double zones

The object of tests was similar to the control system shown in Fig. 3 but in every phase there were two comparators which hysteresis zones were different. The phase current error $\delta_i = i^*(t) - i(t)$ is compared with the set error zones **H** and **SH**, after which the following decision-making procedure is executed:

- if $\lceil \delta_i \rceil < \boldsymbol{SH}$ then the zero vector is activated
- if $\boldsymbol{SH} < \lceil \delta_i \rceil < \boldsymbol{H}$ then the non-zero vector is activated.

So, non-zero vectors are selected when the error exceeds zone SH; once the error turns back into the zone, the zero vector requiring the fewest switch transitions is applied.

A5. Hysteresis algorithm selecting a vector with the longest operation

This algorithm was based on the concept of selecting the inverter output voltage vector with the longest operating time [18]. In this algorithm, the selection of vectors takes place first to reject vectors useless for control at a given phase current error status. Then, after calculating the operating times of the pre-selected vectors with "good direction", the best of them is chosen. The criterion here is the maximum time of staying of the current error vector within the permissible error area. This area has a form of a regular hexagon with side's length equal to *H*.

C. *Simulation results*

Figures from Fig.4 to Fig.9 show the results of simulation studies of individual algorithms in the form of voltage waveforms, currents and vectors. The waveforms obtained in simulation tests of hysteresis algorithms A1 and A2 are shown in Fig.4 while Fig.5 and Fig.6 show printed waveforms of inverter phase currents and voltage vectors obtained in simulation tests of A3 and A4 algorithms. These simulations were obtained for the assumed values of simulation model parameters:

$i^*_{abc}(t)$=$I_m \sin\left(2\pi f t + \frac{2\pi}{3}n\right)$, $e_{abc}(t)$: $E_m \sin\left(2\pi f t + \frac{2\pi}{3}n\right)$
where $n = 0, \pm 1$, φ=45∘ (cos φ=0,7), f=10 Hz
U_D=450 V, E_m=217.5 V, I_m=500 A,
$X2$=0.0382 Ω, $R2$ = 0.068 Ω, SH=6 A, H=10 A, T_p=100 μs

Three next figures, Figs. 7, 8, and 9 show selected examples characterising the properties of the related hysteresis algorithms. These results were obtained for different parameters of the control model.

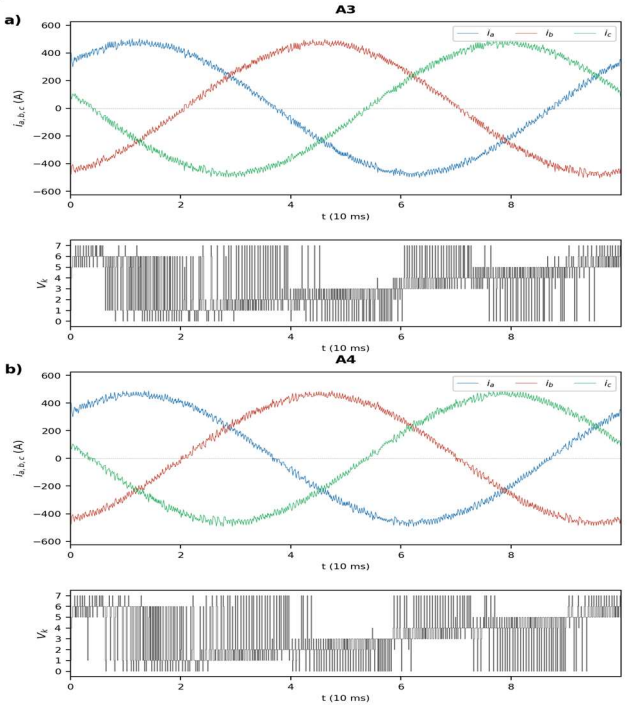

Fig.5. Waveforms of inverter phase currents and voltage vectors for hysteresis algorithms A3 (a) and A4 (b)

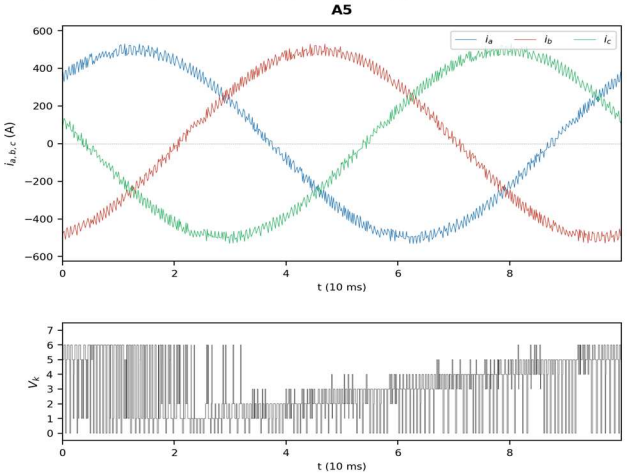

Fig.6. Waveforms of inverter phase currents and voltage vectors for hysteresis algorithm A5

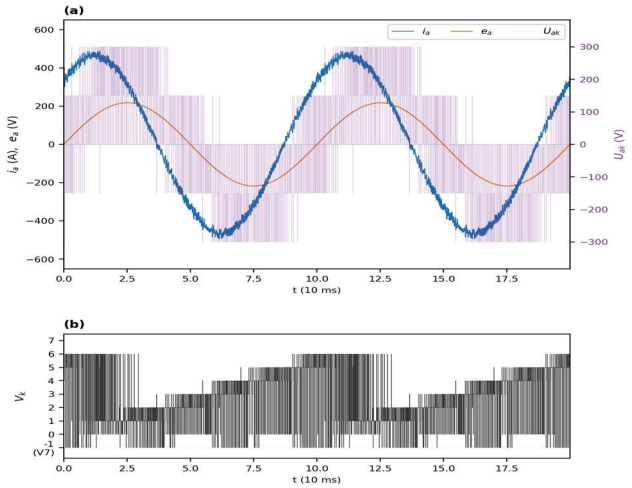

Fig.7. Phase current ia, electromotive force ea, inverter output phase voltage Uak (a), and inverter voltage vectors Vk, (b) obtained for the control model according to the discretized algorithm A5; the assumed sampling period Tp = 100 $\boldsymbol{\mu s}$. (Zero vectors Vk =7(111) marked with number -1).

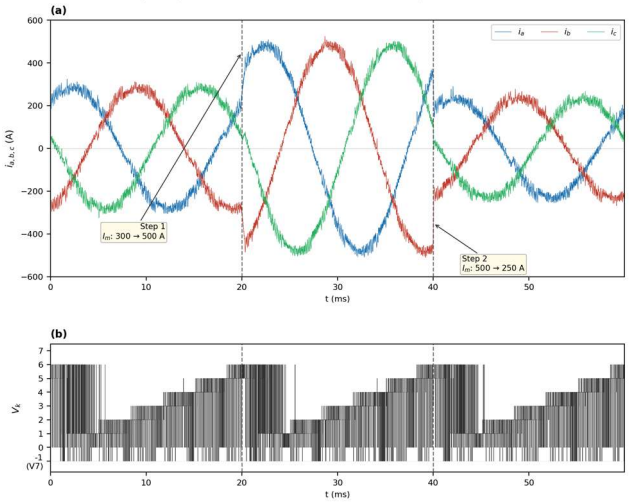

Fig.8. Illustration of dynamic properties of the inverter controlled according to the hysteresis algorithm A1 based on the phase current waveforms obtained at step change of the set value of the current (a), inverter voltage vectors Vk, (b) (zero vectors Vk =7(111) marked with number -1)

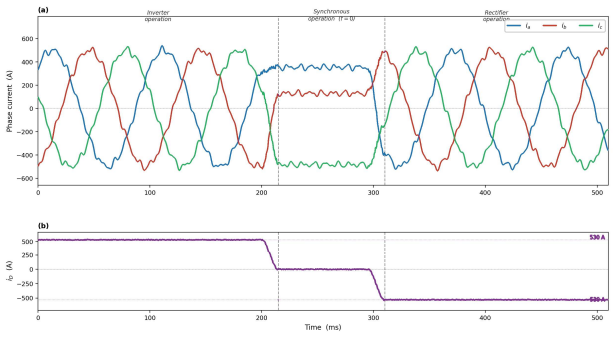

Fig.9. Three modes of converter operation controlled according to algorithm A5: inverter operation, synchronous operation (the set current frequency f = 0), and rectifier operation: (a) three-phase currents, (b) average current value i_D.

The results obtained in the simulation tests are summarised in Table 4. It is noteworthy that the parameter *vnum* included in the table determines the number of converter vector switches. The simulation program increases this number at each vector change. This number is not equal to

the number of terminal switches, as converter switches may occur in which more than one terminal changes state. The obtained results allow the determination of basic properties of the control making use of hysteresis algorithms.

Table 4. Results of simulation tests of algorithms.

Parameter	Algorithm				
	A1	A2	A3	A4	A5
vnum	1344	594	696	549	642
T_{min} T_{max} ϑ	4 μs 192 μs 48	100 μs 700 μs 7	100 μs 500 μs 5	100 μs 700 μs 7	48 μs 372 μs 7.7
T_{av}	74 μs	182 μs	144 μs	182 μs	156 μs
I_D	294.7 A	297.1 A	296.3 A	296.2 A	294.5 A
I_Phase a I_Phase b I_Phase c	352.6 352.6 352.6	345.7 346.3 345.8	345.0 346.5 345.8	345.1 345.8 345.2	353.2 353.6 353.5
THD	0.257%	0.597%	0.539%	0.539%	0.317%

The simplicity in implementation of algorithm A1 is accompanied by good control properties. The algorithm ensures that the current flow is kept within the set limits. It also provides high-speed response to the step change of the set current value. The basic disadvantage of algorithm A1, which eliminates the possibility of its use for controlling the operation of higher-power converters, is the instability of the inverter switching frequency. Very short time intervals between switches may occur, which are beyond physical switching capabilities of the presently used power semiconductor elements. Moreover, quick switches contribute to the increase of the content of higher harmonics in the output current.

The other way to protect against the high switching frequency of converter terminals consists of periodic testing of phase current errors. This method was applied in algorithm A2. As a result, this algorithm does not allow such quick switches as algorithm A1. The converter switching becomes more uniform, and the value of the coefficient ***vnum*** decreases. Compared to algorithm A1, all remaining algorithms have a much smaller ***Tmax/Tmin*** ratio. In this respect, algorithms A3 and A5 look most beneficial. However, algorithm A3 requires a relatively large number of switches, which is most likely related to the obligatory zero vector activation in the zone of auxiliary comparators, without checking the direction of electromotive force.

In all three algorithms A2, A3 and A4, the assumed current sampling frequency f_p = 10 kHz determines the minimum time T_{min} = 100 μs between switches.

For algorithm A5, which, similarly to algorithm A1, allows switching with relatively high frequency, the ratio ϑ = Tmax /Tmin takes a value close to that obtained for periodic algorithms A2 and A4. At the same time, with relatively little variation in switching times, the total number of all switches is larger than for algorithms A2 and A4, which results from allowing for the appearance of switches not synchronized by the sampling frequency.

Only the two aperiodic algorithms ensure keeping the current accurately within the set error zone. If a switching speed limit is introduced to algorithm A5, then achieving such an accuracy becomes impossible. The performed tests have also shown that algorithm A5, at a relatively small number of switches, improves the regularity of converter switching, which is confirmed by the uniformity of loads of individual semiconductor switches, at a much smaller ratio $\vartheta = T_{max} / T_{min}$ compared to algorithm A1.

D. Experimental Tests

The results obtained in simulation tests have been verified practically. The experimental tests were performed on a laboratory model. In the first stage, the object of control was the squirrel cage motor SZJCe 563 6.1 kW, and then, an asynchronous ring motor with power of 50 kW.

The algorithms to be tested were implemented into the control system, the central unit of which was a fixed-point signal processor. For this purpose, the Texas Instruments processor TMS320C25 was selected.

The tests were first performed with the mains converter. The following parameters of the tests were assumed:

$i_{ph}^*(t) = I_M(2\pi ft + \varphi_0)$,

$u_{ph}^*(t) = U_M(2\pi ft + \varphi_0)$, $\varphi_0 = 0, -\frac{2\pi}{3}, +\frac{2\pi}{3}$ $I_M = 20\ A$,

$U_M = 160\ V$, $U_D = 400\ V$, $f = 50\ Hz$.

Load parameters: $L_{ph} = 5\ mH$, $R_{ph} = 1.5\ \Omega$.

Hysteresis zone of the control algorithm: $H = 2\ A$.

The converter was controlled using the dSpace1102 card with synchronization accuracy of 0.011° at 50 Hz. Figs. 10 and 11 show characteristic phase current and voltage waveforms obtained for phase shift angles φ = −π/2, 0, π/2, and π.

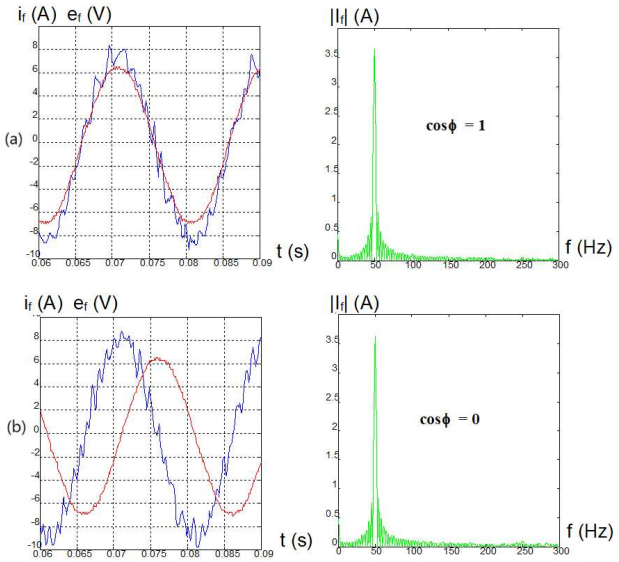

Fig.**10**. Mains converter phase currents and voltages and spectrum of current harmonics for phase shift angle $\varphi = -\frac{\pi}{2}$ (a) and 0 (b)

In the spectra of phase current harmonics, the values of the 3rd harmonic and the 5th harmonic are negligibly small. It can be estimated that their level does not exceed 2% of the fundamental harmonic value. For comparison, in the waveform of the input current of an inverter powered in classic way, the 3rd, 5th and 7th harmonics in the spectrum can reach as much as several dozen percent of the fundamental harmonic.

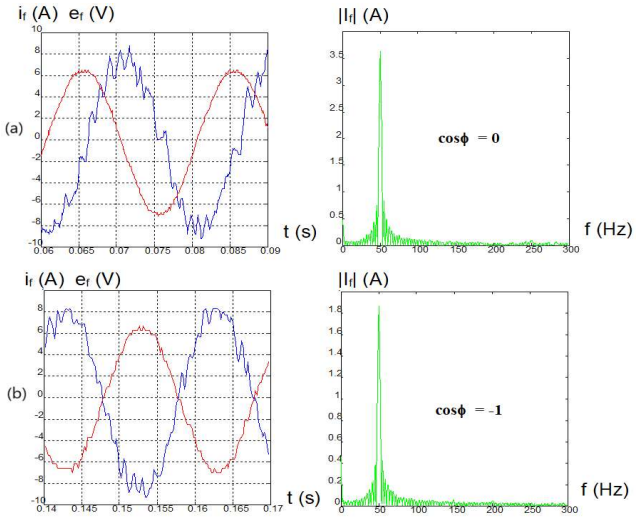

Fig.**11**. Mains converter phase currents and voltages and spectrum of current harmonics for phase shift angle $\varphi = \frac{\pi}{2}$ (a) and π (b)

In the spectra of phase current harmonics, the values of the 3rd harmonic and the 5th harmonic are negligibly small. It can be estimated that their level does not exceed 2% of the fundamental harmonic value. For comparison, in the waveform of the input current of an inverter powered in classic way, the 3rd, 5th and 7th harmonics in the spectrum can reach as much as several dozen percent of the fundamental harmonic.

The experiments were conducted with model based control, in the natural coordinate system of the hysteresis algorithm. The algorithm worked with the shortest possible processing time of the main program loop. The time interruption was set to 65 μs. In object calculations, the algorithm used a linear model, according to the equations presented in Section 2. For the adopted parameters of the experimental model, the number of converter switches did not exceed *vnum* = 50 per one period.

4. Conclusion

The paper has demonstrated the usefulness of a simplified linear model of an AC/DC voltage source inverter operating as a current-controlled grid converter, and has applied this model to a quantitative comparison of five hysteresis control algorithms. The following conclusions can be drawn from the simulation and experimental results. First, the proposed analytical model — derived under the assumption of an ideal switching network and a current-generator equivalent of the DC link — correctly reproduces the steady-state and dynamic behaviour of the inverter across the full range of operation (rectifier, synchronous and inverter modes), as confirmed by the close agreement between simulation and laboratory results. Second, the comparative results in Table 4 indicate that no single algorithm is optimal in every respect. Algorithm A1 (pure analog comparators) gives the lowest THD (0.26 %) and the fastest response to set-point changes, but at the cost of an unbounded switching frequency that exceeds the capability of present-day power semiconductors and an unfavourable T_{max}/T_{min} ratio ($\vartheta \approx 48$). Algorithm A5 (longest-operating-time vector) offers the best balance between THD (0.32 %), switching count and uniformity of semiconductor loading ($\vartheta \approx 7.7$). Algorithms A2–A4, which apply periodic activation of the comparators, are the practical compromise for medium- and high-power applications because they bound the switching frequency at the price of slightly higher harmonic content. Third, the periodic-activation principle introduced in algorithms A2 and A4 — with sampling period chosen on the basis of the load time constant — effectively limits inverter switching frequency without significant deterioration of current control accuracy, provided that the hysteresis zone width is correlated with the sampling period.

Finally, the algorithms were implemented in real time on a Texas Instruments TMS320C25 fixed-point DSP and tested on a 50 kW asynchronous machine, demonstrating that even modest computing hardware is sufficient for production-grade current control of grid-connected VSIs. The proposed model is therefore proposed as a useful design tool for further work on bidirectional energy conversion using current-controlled voltage source inverters.

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